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روش تحقیق کمی

Word نرم‌افزار برای پژوهشگران
New Configuration of Power Electronic Converter for Photovoltaic Systems with a New Inverter Topology

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Abstract—In this paper, a new power electronic converter is suggested for photovoltaic systems. This power electronic conversion system includes a multi-output DC-DC boost converter and a new multilevel inverter topology. This structure uses less number of components such as power switches, gate drivers and diodes. A comparison is drawn between proposed inverter topology, classical and other proposed multilevel inverter topologies to represent the merits of the proposed inverter. Fundamental frequency switching method is presented for triggering power switches. Two different topologies are simulated to confirm the operation of proposed structure through MATLAB/Simulink software.

Keywords—multilevel inverter; fundamental frequency; multi-output DC-DC; boost converter

I. INTRODUCTION

Environmental concerns about reducing fossil fuels, increasing insalubrious gasses and global warming provide the stimulus to research clean energy sources. Solar energy power generation is one of these energy sources which has no air pollution and is an efficient way to generate electricity [1], [2].

Photovoltaic (PV) systems need a power electronics interface in grid-connected or load connected because it converts the dc power generated by solar cell array into ac power [3]. Fig. 1 indicates the basic structure of a PV power conversion system.

In this paper, the challenge is to link the DC generated voltage by the photovoltaic system with output load. DC-DC converters are widely used in renewable energy systems [2]. Recently, various multi-output DC-DC converters have been presented. Multi-output DC-DC converters are more efficient compared to using several separate single output power supplies [4]. In [5], a new multi-output dc–dc boost converter has been presented which can be used as a front-end converter to boost the inverter’s dc link voltage for grid connection system. By adjusting this converter, the dc voltage across each capacitor can be adjusted to a desired voltage level and the main problem associated with balancing the capacitors’ voltages is solved.

Generally, three main structures of the multilevel inverters have been presented: the neutral point clamped (NPC) [6], flying capacitor [7], [8] and cascaded H-bridge (CHB) inverter [9], [10]. The NPC multilevel inverter needs multiple clamping diodes to synthesize the different voltage levels across the output. The main disadvantage of this structure is unbalanced capacitor’s voltage which is used in series to divide up the DC bus voltage into a set of output voltage levels. Also, using more number of diodes and switches is the other disadvantage of this topology. The FC multilevel inverters generate multilevel output voltage waveform based on clamping and balancing capacitors instead of diodes. The FC structure also requires more number of capacitors and switches in high levels and these requirements increase the cost and control complexity for capacitors voltage balancing [11]. The CHB inverter has been considered because it is modular and simple in control. Although this topology is able to generate high levels, it needs more number of switches and gate drivers [12].

Up to now, different multilevel inverter topologies have been submitted in the literature. In [12]-[14], different symmetric cascaded multilevel inverters have been presented. The main disadvantages of these presented topologies are the high required number of power switches, insulated gate bipolar transistors (IGBTs), power diodes and driver circuits.

In this paper, a new topology of symmetric multilevel inverter has been recommended for photovoltaic systems application. This inverter topology is able to generate high level output voltage waveform with the reduced number of power electronic components.

Additionally, various modulation techniques have been presented for multilevel inverters such as selective harmonic elimination (SHE-PWM), sinusoidal pulse width modulation (SPWM), space vector modulation (SVM), Fundamental Frequency Switching and so on [7], [11], [15],
For the presented structure, the fundamental frequency-switching method is used for triggering power switches [13].

II. PROPOSED STRUCTURES

A. First Proposed Structure

Fig. 2 shows the basic configuration of recommended power conversion system. This structure includes a three-output DC-DC boost converter and a basic structure of a new suggested multilevel inverter.

The basic operation and concept of three-output boost converter is completely discussed in [5]. Each capacitor of DC-DC converter has identical values and is given by

\[
\frac{V_C}{V_{in}} = \frac{1}{1 - D}
\]

Where \( V_{in} \) is the input voltage, \( V_1 = V_2 = V_3 = V_C \) are the capacitors voltages and \( D \) is the duty cycle of boost converter which is controlled by switch \( T \) to produce appropriate each capacitor voltage. In this configuration, the three-output boost converter has connected to the suggested seven-level inverter. This multilevel inverter uses 10 IGBTs switches. As this inverter topology is able to generate only positive voltage levels at first section, it is necessary to use an H-bridge inverter for generating negative levels which indicated as a second section in fig. 2. Table I shows the different switches states to generate different seven levels. It is noticeable that there are several switching states for generating zero state and only one of them is shown. In this table, 1 and 0 indicate the ON and OFF states of the switches, respectively.

\[
\begin{array}{cccccccccccc}
\text{States} & S_{1,1} & S_{1,2} & S_a & S'_a & S_2 & S'_2 & T_1 & T_2 & T_3 & T_4 & V_o \\
\hline
1 & 1 & 0 & 0 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & +V_C \\
2 & 1 & 0 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & +2V_C \\
3 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & -V_C \\
4 & 0 & 1 & 0 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & +2V_C \\
5 & 0 & 1 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & -2V_C \\
6 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 1 & 0 & 0 & +3V_C \\
7 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 1 & 1 & -3V_C \\
\end{array}
\]

Fig. 3. Suggested multilevel boost inverter (MLBI).

If \( K (K \geq 3) \) is the number of dc bus capacitors which is generated by DC-DC boost converter, then the number of levels is given by:

\[
N_{level} = 2K + 1
\]

(2)

It is important to note that the dc bus capacitors in fig. 3 are shown as \( V_1, V_2, \ldots, V_K \) in fig. 3.

For this topology, the number of main switches, IGBTs and gate drivers are equal with:

\[
N_{switch} = N_{IGBT} = N_{driver} = 2K + 4
\]

(3)

Considering (2) and (3), the number of IGBTs versus the number of output levels can be calculated as...
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B. Second Proposed Structure

For generating more number of levels with less number of power electronic elements, cascaded multilevel inverter can be used. The number of power electronic elements versus the number of output voltage waveform levels defines the complexity, cost and reliability. Also, increasing the number of dc bus capacitor’s voltage to generate more number of levels makes difficulties in balancing. Therefore, to prevent these problems, a three level inverter has been cascaded with basic structure, which is indicated in fig. 4. It is noticeable that the magnitude of all capacitors is equal to \( V_1 = V_2 = \ldots = V_K = V_C \).

If \( V_b \) represent the magnitude of output voltage of multi-output boost converter, then to generate more number of levels, the amount of dc voltage source of three level inverter is given by the following equation

\[
V_T = \frac{V_b}{2K}
\]  
(5)

or

\[
V_T = \frac{V_C}{2}
\]  
(6)

In this equation, \( K \) is the number of dc bus capacitors with multi-output converter generate.

For the suggested structure, the control switches is important. By controlling duty cycle of switch \( T \), the value of capacitor’s voltage of multi-output boost DC-DC converter can be adjusted [5]. For recommended multilevel inverter topology, the control of switches has been done by utilizing fundamental frequency switching technique [13]. One of the most important indexes in inverter’s performance is total harmonic distortion (THD) [13], which given by:

\[
THD = \sqrt{\frac{\sum_{m=3,5,\ldots}^{n} V_{o,m}^2}{V_{o,1}}}
\]

\[
= \left( \frac{V_{o,rms}}{V_{o,1}} \right)^2 - 1
\]  
(11)

With respect to (5) or (6) and fig. 4, the number of levels and switches, IGBTs and gate drivers can be detected as (7) and (8), respectively:

\[
N_{\text{level}} = 4m - 1
\]  
(7)

\[
N_{\text{switches}} = N_{\text{IGBT}} = N_{\text{driver}} = 2m + 6
\]  
(8)

where \( m \) denote the number of all dc bus voltages containing multilevel inverter and three level inverter i.e. (number of \( V_1, V_2, \ldots, V_K \) and \( V_T \) ) and given by

\[
m = K + 1
\]  
(9)

By combination of (7) and (8), we can calculate the number of IGBTs and drivers versus the number of levels as

\[
N_{\text{IGBT}} = \frac{N_{\text{level}} + 13}{2}
\]  
(10)

### TABLE II. COMPARISON SUGGESTED TOPOLOGY WITH CLASSICAL MULTILEVEL INVERTERS AND OTHER PRESENTED TOPOLOGIES IN [12]-[14]

<table>
<thead>
<tr>
<th>Topology</th>
<th>Power electronic components</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clamping diode</td>
<td>Balancing capacitor</td>
</tr>
<tr>
<td>Diode clamped</td>
<td>((n-1) \times (n-2))</td>
</tr>
<tr>
<td>Flying capacitor</td>
<td>((n-1) \times (n-2)/2)</td>
</tr>
<tr>
<td>Cascaded H-bridge</td>
<td>0</td>
</tr>
<tr>
<td>Presented topology in [12]</td>
<td>0</td>
</tr>
<tr>
<td>Presented topology in [13]</td>
<td>0</td>
</tr>
<tr>
<td>Presented topology in [14]</td>
<td>0</td>
</tr>
<tr>
<td>First proposed topology</td>
<td>0</td>
</tr>
<tr>
<td>Second proposed topology</td>
<td>0</td>
</tr>
</tbody>
</table>

III. SWITCHES CONTROL

For the suggested structure, the control switches is important. By controlling duty cycle of switch \( T \), the value of capacitor’s voltage of multi-output boost DC-DC converter can be adjusted [5]. For recommended multilevel inverter topology, the control of switches has been done by utilizing fundamental frequency switching technique [13]. One of the most important indexes in inverter’s performance is total harmonic distortion (THD) [13], which given by:

Fig. 4. Recommended cascaded boost inverter.
where \( V_{o,m} \) is the rms of the \( m \) order component of the output voltage. \( V_{o,rms} \) and \( V_{o,1} \) being the rms values of the output voltage and the fundamental of the output voltage, respectively. The amount of \( V_{o,rms} \) and \( V_{o,1} \) are computed using the following equation, respectively.

\[
V_{o,rms} = \frac{2\sqrt{2}V_b}{\pi} \sqrt{\sum_{m=1}^{\infty} \left( \sum_{i=1}^{N_{\text{level}}} \cos(m\theta_i) \right)^2 }
\]

(12)

\[
V_{o,1} = \frac{2\sqrt{2}V_b}{\pi} \sum_{i=1}^{N_{\text{level}}} \cos(m\theta_i)
\]

(13)

where the parameters \( \theta_1, \theta_2, \ldots, \theta_{N_{\text{level}}} \) are switching angles and given by the following equation:

\[
\theta_i = \sin^{-1}\left(\frac{i - 0.5}{N_{\text{level}}}\right), \quad i = 1, 2, \ldots, N_{\text{level}}
\]

(14)

### IV. SIMULATION RESULTS AND ANALYSIS RESULTS

To verify the performance of designed MLBI, MATLAB/Simulink software simulation has been done for two different structures. The parameters used in simulations are listed in table III.

#### A. Four-Output DC-DC Boost Converter Linked to Nine-Level Inverter

Fig. 5 indicates a four-output boost converter which connected to a nine-level inverter without cascading three-level inverter. This inverter topology consists of 12 IGBTs and drivers circuits. This Inverter topology is able to generate nine levels (4 positive levels, 4 negative levels, and 1 zero level) with the maximum voltage of 200 V.

Table IV indicates the look-up table of switches states for nine-level boost inverter.

![Fig. 5. Structure of nine-level boost inverter.](image)

![Fig. 6. Input voltage and balanced voltage of each capacitors for four-output boost converter.](image)

### TABLE IV. SWITCHES STATES TO GENERATE DIFFERENT NINE-LEVELS

<table>
<thead>
<tr>
<th>States</th>
<th>( S_{1,1} )</th>
<th>( S_{1,2} )</th>
<th>( S_{2,1} )</th>
<th>( S_{2,2} )</th>
<th>( S_{3,1} )</th>
<th>( S_{3,2} )</th>
<th>( T_1 )</th>
<th>( T_2 )</th>
<th>( T_3 )</th>
<th>( V_o )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>+50</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>-50</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>+100</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>-100</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>+150</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>-150</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>+200</td>
</tr>
<tr>
<td>8</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>-200</td>
</tr>
<tr>
<td>9</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

### TABLE III. USED PARAMETERS IN SIMULATIONS

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltages ( (V_{in} \text{ and } V_T) )</td>
<td>25 V</td>
</tr>
<tr>
<td>Capacitor ( (C) )</td>
<td>100 ( \mu )F</td>
</tr>
<tr>
<td>Inductor ( (L) )</td>
<td>1.5 mH</td>
</tr>
<tr>
<td>Duty cycle ( (T) )</td>
<td>0.5</td>
</tr>
<tr>
<td>Fundamental frequency</td>
<td>50 Hz</td>
</tr>
<tr>
<td>Switching frequency for DC-DC boost converter</td>
<td>15 KHz</td>
</tr>
<tr>
<td>Resistive load</td>
<td>50 ( \Omega )</td>
</tr>
<tr>
<td>Inductive load</td>
<td>10 mH</td>
</tr>
</tbody>
</table>
Fig. 7 indicates the nine-level inverter outputs after transient state in two cycles. Fig. 7 (a) and (b) shows the output voltage and output current with their relative Fast Fourier Transform (FFT) analysis, respectively.

FFT analysis shows that the THD of output voltage and output current are 9.22% and 5.89%, respectively. The FFT analysis indicates that the magnitudes of harmonics of both voltage and current waveforms are low. However, the harmonics of the current waveform are lower than the voltage waveform. It is noticeable that, for decreasing the magnitudes of harmonic components, LC filter can be utilized.

**B. Three-Output DC-DC Boost Converter Connected to Fifteen-Level Inverter**

To indicate more performance of the suggested structure, a three-output boost converter with fifteen-level inverter which cascaded with a three-level inverter is simulated and is shown in fig. 8. Table V shows the look-up of switches states for the fifteen-level boost inverter.

![Fifteen-level cascaded boost inverter](image)

**TABLE V. VALUES OF $V_o$ FOR DIFFERENT STATES OF THE SWITCHES.**

<table>
<thead>
<tr>
<th>States</th>
<th>$S_{1A}$ $S_{1B}$</th>
<th>$S_{2A}$ $S_{2B}$ $T_1$ $T_2$ $T_3$ $T_4$ $T_5$ $T_6$</th>
<th>Output Voltage ($V_o$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1 1 0</td>
<td>0 0 1 0 1 0 0</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>1 0 0</td>
<td>1 1 0 1 0 1 1</td>
<td>+25</td>
</tr>
<tr>
<td>3</td>
<td>1 0 0</td>
<td>0 0 1 0 0 0 0</td>
<td>-25</td>
</tr>
<tr>
<td>4</td>
<td>1 0 0</td>
<td>0 1 0 0 0 1 1</td>
<td>+50</td>
</tr>
<tr>
<td>5</td>
<td>1 0 0</td>
<td>1 0 1 1 1 0 0</td>
<td>-50</td>
</tr>
<tr>
<td>6</td>
<td>1 0 0</td>
<td>0 1 1 1 1 1 1</td>
<td>+75</td>
</tr>
<tr>
<td>7</td>
<td>1 0 0</td>
<td>1 0 0 0 0 0 0</td>
<td>-75</td>
</tr>
<tr>
<td>8</td>
<td>0 1 0</td>
<td>0 1 1 1 1 0 0</td>
<td>+100</td>
</tr>
<tr>
<td>9</td>
<td>0 1 0</td>
<td>0 1 0 0 0 1 0</td>
<td>-100</td>
</tr>
<tr>
<td>10</td>
<td>0 1 0</td>
<td>0 1 1 1 1 1 0</td>
<td>+125</td>
</tr>
<tr>
<td>11</td>
<td>0 1 0</td>
<td>1 0 0 0 0 0 0</td>
<td>-125</td>
</tr>
<tr>
<td>12</td>
<td>0 1 0</td>
<td>0 0 1 1 1 1 1</td>
<td>+150</td>
</tr>
<tr>
<td>13</td>
<td>0 1 0</td>
<td>1 0 0 0 0 1 1</td>
<td>-150</td>
</tr>
<tr>
<td>14</td>
<td>0 1 0</td>
<td>0 1 0 0 0 0 0</td>
<td>+175</td>
</tr>
<tr>
<td>15</td>
<td>0 1 0</td>
<td>0 1 1 1 1 1 1</td>
<td>-175</td>
</tr>
</tbody>
</table>

Fig. 7. Nine-level inverter outputs; (a) Output voltage and it’s FFT analysis (THD=9.22%), (b) Output current and it’s FFT analysis (THD=5.89%).
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The simulated output voltage and current waveforms are shown in Fig. 9. The THD of the output voltage and current waveforms are 5.42% and 2.57%, respectively. Comparing the output voltage and current waveforms indicates that the output current waveform is more similar to the ideal sinusoidal waveform than the output voltage because the R–L load acts as a low-pass filter.

Also, Fig. 10 shows the waveforms of input voltage source \(V_{in}\) and balanced voltages of boost converter’s capacitors. The amount of capacitor’s voltage is almost 50V. As can be seen, by cascading three-level inverter, the balancing of capacitor’s voltages of the multi-output boost converter is held fixed without changing.

V. CONCLUSION

This study presented a new structure of power electronic converter for photovoltaic applications. A multi-output DC-DC boost converter was used to provide several self-balanced voltage levels and only one driven switch. Also, a new multilevel inverter topology is proposed and then to reduce costs, control complexity and increasing reliability, the proposed topology inverter is modified by cascading three-level inverter. Then, both proposed topologies compared with conventional multilevel inverters and other multilevel inverter topologies to reveal advantages of recommended inverter topology. Fundamental frequency switching strategy is utilized to turn on and turn off inverter switches. Finally, two different structures including four-output boost converter linked to nine-level inverter and three-output converter linked to fifteen-level inverter simulated to verify performance of the structure.

REFERENCES


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