RESEARCH NOTE

A VERY LOW VOLTAGE 9TH ORDER LINEAR PHASE BASEBAND SWITCHED CAPACITOR FILTER

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(Received: June 23, 2003 – Accepted in Revised Form: December 25, 2003)

Abstract  A very low voltage 9th order linear phase baseband switched capacitor (SC) filter has been designed to be used as part of a cellular GSM (Global System Mobile) receiver. A Gaussian-to-6dB filter of the order of seven is chosen and a second order function is added to reduce the group delay variations around 1MHz. The filter uses a fully digital topology to increase the dynamic range and reduce the clock feed-through noise and the distortion due to low voltage amplifier. Using a chopper stabilization technique in opamp design reduces the flicker noise. In order to reduce the charge injection two methods of delayed clock phases and dummy switches are used. The filter is realized by cascading the biquad sections. The filter has been designed in a 0.35µm CMOS technology and simulated with Hspice using BSIM 3V3 model. The filter operates at 2MHz sampling frequency and 1MHz chopping frequency with a corner frequency of 100 KHz and 7 mW power consumption.

Key Words  Low Voltage Analog Circuit, Baseband SC Filter

1. INTRODUCTION

Baseband filters are the essential blocks in modern cellular telephone receivers, providing a significant amount of the adjacent channel selectivity and thus improving the S/N ratio or the bit error rate. Two techniques are commonly employed to implement the filtering function: continuous-time and switched capacitor. Based on the receiver architecture the filter can be a band pass or low pass. If the filter is used in the second-IF section it must be a band pass filter and if used in zero-IF, it must be a low pass one. Under the same channel bandwidth condition, the low pass filter (LPF) with respect to the band pass one has a lower Q factor. The Q factor control loops are not needed in base band LPF due to its lower Q.

The time constants in SC filter integrators are a
function of reference clock frequency and the ratio of the capacitor values, which both can be well controlled. Thus the SC approach has the potential of presenting the filter transfer function largely process independent.

The requirements for the baseband filter characteristics are derived from spectral density profile of a GSM modulated signal. Based on the above information the filter corner frequency must be 100KHz with in-band group delay variations up to \( 1 \mu s \). Based on the worst-case signal frequency, which passes through the SCF, the filter output slew rate and hence the opamp slew rate must be \( 3.2V/\mu s \). Thus, a 7th order Gaussian-to-6dB characteristics is chosen due to its desired constant group delay within the passband, minimal signal dispersion, minimum intersymbol interference, and stopband steep attenuation slope. Minimizing the intersymbol interference requires that group delay variations within the data bandwidth be lower than the GSM index interval, which is \( 7.3\mu s \). This can be achieved by adding a 2nd order all pass function to the above 7th order transfer function and choosing its proper pole-zero values, the group delay within the required frequency range is reduced to less than \( 1 \mu s \).

Due to low voltage power supply, the available MOS overdrive voltage required for switching action is reduced and classical methods of complementary switches (transmission gates) are no longer effective. Thus, to overcome this problem wherever critical (i.e. where varying signals or reference voltages are switched), bootstrapped switches are used.

The low voltage requirements of the circuit results in reduced opamp dynamic range, considerable noise due to the clock feed-through, and amplifying distortion. Using fully differential amplifiers the above problems are reduced considerably.

2. FILTER STRUCTURE

In order to implement the 9th order transfer function of the filter, four biquad sections as well as a single pole section are cascaded. Since the transfer function of the composite filter is the product of poles and zeros of all cascaded biquads, it is independent of pole-zero pairings and biquad orderings. However in order to maximize S/N ratio of all internal nodes within the passband the pairing and ordering are needed. This is done by using the available optimization algorithms for decomposition of the composite filters such as internal S/N ratios maximized [5].

The biquad integrator capacitor scaling is performed to maximize the dynamic range (DR), and to minimize the total capacitance of the filter, where in the latter scaling the minimum unit capacitor is chosen to be 0.25pF. The effective factors in choosing this unit capacitor include: die area, capacitor spread, capacitance error due to routing or process matching limitations, and the desired noise level of the filter. The required algorithms for the above optimizations, which have to be done respectively, can be found in references [3,4]. Figure 1 shows the single pole section, which is placed, as the first section in the biquad chain. A general form of the differential biquad structure used in cascaded sections is shown, in Figure 2. The single pole section is a continuous-time lossy inverting integrator mapped with backward-Euler transformation (instead of bilinear) since this results in a parasitic-insensitive structure [3,7]. In Table 1 the capacitive values of each cascaded section are listed.

3. OPAMP DESIGN

In Figure 3 the proposed fully differential opamp is shown. This opamp is a two stage Miller compensated topology. Since the opamp input and output common mode (CM) voltage levels are not the same, in order to use the opamps in biquad integrator chain a double voltage reference scheme as shown in Figure 2 is used to compensate this CM voltage difference.

The common mode feedback (CMFB) circuit is provided for each stage separately, which eliminates the need for an extra inverting CMFB amplifier [1].

Due to the cross-coupled transistor connections in the first stage, the minimum supply voltage for the opamp is \( V_{GS} + V_{DSSat} \). In Table 2 the opamp simulated performance results are shown.
4. BOOTSTRAPPED SWITCH

Figure 4 shows the structure of the bootstrapped switch. The main switch is the MNSW transistor, which its gate has been bootstrapped. During $\phi_n$, the pre-charged capacitor $C_{\text{offset}}$ which previously...
has been charged to VDD is placed between MNSW gate and source and thus in all cases switch provides rail-to-rail operation.

The advantage of this switch with respect to others is that its reliability problems are considered under both low voltage and transient states of the switch [2]. In order to reduce the number of bootstrap switches, the ones in sampling network which connect the output of integrator to the next stage can be shared with the CMFB network as shown in Figure 2.

### TABLE 1. Capacitor Values of Each Section (pF).

<table>
<thead>
<tr>
<th>Pole</th>
<th>Single 1(^{st}) biquad</th>
<th>2(^{nd}) biquad</th>
<th>3(^{rd}) biquad</th>
<th>4(^{th}) biquad</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0</td>
<td>0.25</td>
<td>1.601</td>
<td>2.573</td>
</tr>
<tr>
<td>B</td>
<td>0</td>
<td>1.083</td>
<td>0.793</td>
<td>5.895</td>
</tr>
<tr>
<td>C</td>
<td>0.25</td>
<td>0.25</td>
<td>0.25</td>
<td>0.587</td>
</tr>
<tr>
<td>D</td>
<td>1.635</td>
<td>0.470</td>
<td>7.781</td>
<td>1.250</td>
</tr>
<tr>
<td>E</td>
<td>0</td>
<td>0.410</td>
<td>0</td>
<td>0.25</td>
</tr>
<tr>
<td>F</td>
<td>0</td>
<td>0</td>
<td>0.265</td>
<td>0</td>
</tr>
<tr>
<td>G</td>
<td>0.25</td>
<td>0.25</td>
<td>0.25</td>
<td>0.486</td>
</tr>
<tr>
<td>J</td>
<td>0</td>
<td>0</td>
<td>0.25</td>
<td>0</td>
</tr>
<tr>
<td>K</td>
<td>0</td>
<td>0</td>
<td>0.4</td>
<td>0.25</td>
</tr>
</tbody>
</table>

\[ \Sigma \text{Cap} = 2.135 \times 2 \quad 2.713 \times 2 \quad 11.59 \times 2 \quad 11.291 \times 2 \quad 2.667 \times 2 \]

### Table 2. Opamp Simulated Performance Results.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>1V</td>
<td>slew rate</td>
<td>3.37V/μs</td>
</tr>
<tr>
<td>GBW</td>
<td>25MHz</td>
<td>load Cap</td>
<td>4pF</td>
</tr>
<tr>
<td>PM</td>
<td>80 Deg</td>
<td>Comp Cap</td>
<td>14pF</td>
</tr>
<tr>
<td>DC Gain</td>
<td>70dB</td>
<td>Power Dis.</td>
<td>0.78mW</td>
</tr>
<tr>
<td>Output Swing</td>
<td>0.15-0.85V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 5. NOISE AND CHARGE-INJECTION REDUCTION

In order to reduce the input and output noise, the optimization of the input opamp noise is an important stage of the design. Using higher input current in the input differential pair can reduce thermal noise. The flicker noise can be reduced by chopper stabilization technique [1]. Input chopping is done by four switches in opamp input as shown in Figure 2, where \( \phi_{b1} \) and \( \phi_{b2} \) are clock phases to drive chopper switches. The output chopping is done in the output of the opamp's first stage using M31-2 and M41-2 transistors, rather than the output of the second stage. Chopping clock phases must overlap to avoid turning off these switches simultaneously. This causes an increase in the settling time of the opamp. These phases must also

![Opamp Structure](image-url)
be stable during the transient states of the sampling clock phases.

During the switch turn-off time, charge injection is a serious problem in SC circuits. For switches, which transfer large varying signals, channel charges are modulated by the signal and thus introduce a signal dependent distortion. However, utilizing the bootstrap switches reduces this effect by keeping the switch gate-source voltage independent of the signal. In addition, using delayed clock phases reduces the charge injection even further. Applying this technique, the maximum integration error due to charge injection is limited to transistor S4 that is connected to summing node of the integrator directly. Due to the presence of the clock pulse, approximately half of the S4 channel charge flows into this node, which introduces clock feed-through and DC offset due to sampling aliasing. A solution to this problem is to introduce a dummy transistor (Mdum in Figure 2) with its drain and source terminals connected together (only gate to channel capacitance is needed) and the gate area is half the S4 gate area. This transistor is clocked with S4's complementary clock phase.

6. SIMULATION RESULTS

The filter is designed and simulated in 0.35\(\mu\)m CMOS technology with \(V_{thp} = 0.62V\) and \(V_{thn} = 0.51V\) using Hspice with BSIM 3V3 model. The achieved results are shown in Table 3. The sampling frequency is 2MHz and opamp input-output chopping frequency is 1MHz. In Figure 5, the filter overall amplitude response as well as 4 biquad and one single pole responses are shown. The phase response with respect to ideal continuous time state is presented in Figure 6. The small deviation in the phase response is due to the usage of backward-Euler mapping in the single pole stage, which has been utilized because of its insensitivity to parasitic elements.

7. CONCLUSION

SC technique has been applied to design a 9th order baseband linear phase filter to be used as a
part of GSM cellular telephone receiver. The focus of this design was to solve the problems in switches and opamps due to operation in very low voltage regimes while reducing the noise and distortion effects.

8. REFERENCES


