Class-AB Square-Root Domain Filters Based on the Floating Gate MOS Translinear Principle

E. Farshidi* and S. M. Sayedi*

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Keywords: Companding Filter, Current-Mode, Geometric-Mean, Square-Root-Domain.

1 Introduction
The trend towards portable electronic computing, communication and entertainment equipment, which mostly operate by battery, has increased the interest of researches in very low voltage and low power companding (compressing/expanding) circuits. In a filter that employs companding technique, the input signals which are mostly in current domain are nonlinearly transformed to the compressed voltage signal domain, the processing is done nonlinearly in this voltage domain and then the compressed output voltage is transformed back into the current domain. Therefore, in spite of the fact that the voltage nodes are internally nonlinear the input/output relation is linear. Taking advantage of the companding principle, log-domain filters were introduced by Adams in 1979 [1] and later formulated by Frey in 1993 [2]. The first implementation of log-domain circuits employed the exponential I-V characteristic of the bipolar transistors [3]. Developments in CMOS circuits and also similarity in I-V characteristics, caused the bipolar transistors were substituted by MOS transistors working in weak inversion region [4]. Despite advantages of these circuits, the effects of limited speed and transistor mismatches restricted their applications. Afterwards, companding systems employed MOS transistors, working in saturation region based on voltage translinear loops [6-10] and class-AB linear transconductors [5], which led to class-A Square-Root-Domain (SRD) structures. The main drawbacks of these proposed structures are as follows: first, the body effect of the stacked translinear loop [6, 7] and class-AB transconductors circuits [5] decrease the accuracy of the system, influence of the body effect in up-down translinear loop [8-10] is smaller than in stacked loop but the circuit complexity of up-down translinear loop is higher; secondly, these SRD filters operate in class-A topology, thus the needed extra biasing currents and voltages increase static power consumption; and finally, in these circuits employing low voltage restricts input dynamic range [4-10]. In this work, to overcome the above problems, FG-MOS transistors with sources connected to the substrate are employed to construct the electronically translinear loop circuit of SRD filters. The proposed filters are immune to the body effect and the circuit complexity is much less than those proposed before [5-10]. Other advantages of these filters are that, these circuits operate in class-AB, so extra biasing currents and voltages are not needed, very low voltage with minimum of one $V_{gs}$ plus one $V_{ds}$ is required and the dynamic range is much wider than those proposed before [6-10].

The paper is organized as follows. In Section 2 the analysis of current-mode SRD integrator and two examples of class-A SRD filter are discussed. In Section 3 design of geometric-mean circuit as one of the building blocks of the filters is presented. Section 4 explains the class-AB SRD filters. Simulation results are presented and discussed in Section 5 and concluding remarks are provided in Section 6.
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2 SRD current-mode filters

2.1 Analysis of SRD class-A integrator

In general, implementation of a high-order filter requires the use of multi-input integrators driven by either external input current or internal state-space variable currents. The linear differential equation of the integrators in current domain is expressed by:

\[
d\frac{I_n}{dt} = \frac{1}{\tau_n} \left( \sum_{k=1}^{K_1} I_{n_1} - \sum_{k=2}^{K_2} I_{n_2} \right)
\]

in which \(I_{n_1}\) and \(I_{n_2}\) are the positive and negative input currents of the integrator and are either internal state-space variables or external input currents, \(I_n\) is the output current of the integrator, \(K_1\) and \(K_2\) are the number of positive and negative input currents and \(\tau_n\) is the general time constant of the integrator. Figure 1 shows the block diagram of the integrator according to (1).

To design the circuit of the current-mode integrator we start with the analysis of the circuit shown in Fig. 2. Assuming that transistor M1 is in saturation region, current \(I_n\) is nonlinearity related to a capacitor voltage \(V_{cap,n}\) by:

\[
I_n = K \left( V_{cap,n} - V_{th} \right)^2
\]

where, \(K = \mu C_{ox} W / L\) is the tranconductance parameter and \(V_{th}\) is the threshold voltage of transistor M1.

Derivation of (2) and using equation \(I_{cap,n} = C_n \frac{dV_{cap,n}}{dt}\) gives:

\[
d\frac{I_{cap,n}}{dt} = 2\sqrt{K} I_n \frac{dV_{cap,n}}{dt} \Rightarrow
\]

\[
I_{cap,n} = \frac{C_n}{2\sqrt{K} I_n} \times \frac{dI_n}{dt}
\]

Considering current \(I_n\) as the output current of the integrator and using (1) in (3) results:

\[
I_{cap,n} = \sqrt{I_{n_1}} \left( \sum_{k=1}^{K_1} I_{n_1} - \sum_{k=2}^{K_2} I_{n_2} \right)
\]

in which \(I_{bn}\) as the input bias of the integrator is defined by:

\[
I_{bn} = \frac{C_n^2}{4K\tau_n^2}
\]

Equation (4) can be rewritten as:

\[
I_{cap,n} = \sqrt{\sum_{k=1}^{K_1} I_{n_1}^2} - \sqrt{\sum_{k=2}^{K_2} I_{n_2}^2}
\]

In implementation of Eq. (6) it should be noted that, the summation of currents in both right hand side (RHS) terms of Eq. (6) can be done simply by employing two summing nodes based on the KCL law and that the two RHS terms of Eq. (6) are similar and can be expressed by following operator:

\[
\sqrt{I_xI_y} = \sqrt{I_x} \sqrt{I_y}
\]

This operator can be implemented by cascading of a squarer/divider circuit \(I_x^2/I_y\) with input currents \(I_x\), \(I_y\) and a geometric-mean circuit \(\sqrt{(I_x^2/I_y)}\) with input currents \(I_x\) and \(I_y^2/I_y\). The advantage of this cascading of inverse functions is its ability to make non-linearity compensation. Figure 3 shows the block diagram of the integrator which consists of two geometric-means, two squarer/dividers, a capacitor, a current mirror (M3C, M4C) and two MOS transistors M1C and M2C for nonlinear conversion of voltage to current.

Fig. 1 Block diagram of the current-mode integrator.

Fig. 2 SRD integrator principle.
2.2 Examples of class-A SRD filters

This section employs the proposed integrator for two different filters.

2.2.1 First-Order low-pass SRD filter

For a current-mode first-order low pass filter output current $I_{out}(s)$ and input current $I_{in}(s)$, in Laplace domain, are related as:

$$\frac{I_{out}(s)}{I_{in}(s)} = \frac{1}{1 + \frac{s}{\omega_c}}$$

where $\omega_c$ is cut-off frequency of the filter. In time domain Eq. (8) can be written as:

$$\frac{dI_{out}}{dt} = \frac{1}{\tau}(I_{in} - I_{out})$$

in which, $\tau = 1/\omega_c$ is time constant of the filter. Figure 4 shows the general block diagram of the current-mode first-order filter. Applying the derived equations (5) and (6) of Fig. 1 to Fig. 4 results:

$$I_{cap} = \sqrt{\frac{I_{in}}{I_{out}}} - \sqrt{\frac{I_{out}}{I_{in}}}$$

$$I_b = \frac{C^2}{4K\tau}$$

The cut-off frequency of the filter can be written as:

$$\omega_c = 2\sqrt{K/C}$$

Equation (12) shows that the frequency response of the filter is tuneable by changing either the tuning current $I_b$ or the value of capacitor.

2.2.2 Second-Order low-pass SRD filter

The transfer function of a second-order filter is given by:

$$H(s) = \frac{I_{out}(s)}{I_{in}(s)} = \frac{1}{1 + \tau_1s + \tau_1\tau_2s^2}$$

in which $\tau_1$, $\tau_2$ are time constants of the filter. The state-space equations of Eq. (13) in current-mode are as follows:

$$\begin{align*}
\frac{dI_1}{dt} &= \frac{1}{\tau_1}(I_{in} - I_{out}) \\
\frac{dI_2}{dt} &= \frac{1}{\tau_2}(I_{in} - I_{out})
\end{align*}$$
where current $I_1$ is the internal state-space variable. Figure 5 shows the block diagram of the filter based on Eq. (14). Using Eq. (15), the input biases of the two integrator blocks of the figure are defined by:

$$I_{b1} = \frac{C_1^2}{4K_1}, \quad I_{b2} = \frac{C_2^2}{4K_2^2} \quad (15)$$

Second-order systems are usually described by their natural frequency $\omega_0$ and quality factor $Q$ as:

$$\omega_0 = \frac{1}{\sqrt{\tau_1 \tau_2}}, \quad Q = \frac{1}{\sqrt{\tau_2}} \quad (16)$$

Using Eq. (15) into (16) gives:

$$\omega_0 = \frac{1}{nUT \sqrt{C_1C_2}}, \quad Q = \frac{I_{b1} \times C_2}{I_{b2} \times C_1} \quad (17)$$

From (17) it is evident that the natural frequency and quality factor of the second-order SRD filter can be tuned independently.

### 2.3 Class-AB SRD filters

In class-A filters, the input current $I_{in}$ is limited by the current bias $I_{ref}$ ($I_{in} < I_{ref}$). Also, static power consumption, even during absence of the input signal, is considerably high. In class-AB filters, with positive and negative input currents, the bias currents are not needed. This increases the dynamic range of the filter and also reduces the static power consumption. Figure shows the general approach for implementation of the class-AB current-mode filters. It presented in [12-14] for log-domain filters and is adopted in our present work for SRD filters.

As the figure shows, input current $I_{in}$ is split into two currents $I_{inp}$ and $I_{inn}$ by a current splitter. These two currents are strictly positive and processed by two separate class-A signal paths. The resulting currents $I_{outp}$ and $I_{outn}$ are subtracted to obtain the output of the filter.

![Fig. 5 Block diagram of the second-order low pass filter.](image)

![Fig. 6 Block diagram of current-mode class-AB filters.](image)
Thus, the drain current of an FG-NMOS transistor with $N$ input gates, in saturation region is given by:

$$I_d = K(N \sum_i w_i (V_i - V_{th})^2)$$ (21)

where $w_i$ is the $i$-th input capacitance ratio defined as:

$$w_i = \frac{C_i}{C_t}$$ (22)

### 3.2 Geometric-Mean circuit

The geometric-mean circuit block as the basic block of the proposed filters can be implemented by using of translinear [6-10] or class-AB tranconductance [5] circuits. MOS translinear circuits can be categorized as follows: stacked loop, up-down loop and electronically simulated loop [11]. The stacked loop circuit [6-7] similar to class-AB tranconductance circuit suffers from body effect. Placing the transistors in separate wells can eliminate the body effect, but the large parasitic well-to-substrate capacitances will slow down the speed of the circuit. The body effect in up-down loop circuit [8-10] is smaller but it needs more circuitry for current injection into transistors.

In this paper for implementation of the geometric-mean circuit an electronically simulated translinear loop based on FG-MOS transistors is employed. The complexity of this category is much lower than up-down circuits.

Figure 8 shows the basic circuit of the proposed translinear loop. It consists of three FG-MOSs, and it is assumed that all transistors are operating in saturation region. The sources of transistors in the loop are grounded so the effect of the body effect is completely eliminated.

The I-V relationships for transistors M1, M2 and M3 are given by:

$$I_1 = K_1 (w_{11} V_1 + w_{12} V_1 - V_{th})^2$$ (23)

$$I_2 = K_2 (w_{21} V_2 + w_{22} V_2 - V_{th})^2$$ (24)

$$I_3 = K_3 (w_{31} V_3 + w_{32} V_2 - V_{th})^2$$ (25)

Assuming that $K_3 = 4K_1 = 4K_2$ and $w_{11} = w_{12} = w_{21} = w_{22} = w_{31} = w_{32} = 1/2$, from equations (23), (24) and (25) the following expression will be obtained

$$I_3 = I_1 + I_2$$ (26)

Squaring both sides of (26) results:

$$I_3 = I_1 + I_2 + 2\sqrt{I_1 I_2}$$ (27)

If the injecting current of transistor M3 is such that:

$$I_3 = 2I_{g-m} + I_1 + I_2$$ (28)

then, for a certain current $I_{g-m}$ we have:

$$I_{g-m} = \sqrt{I_1 I_2}$$ (29)

Therefore, a geometric-mean circuit is obtained if we use $I_1$ and $I_2$ as the input currents and use a copy of $I_{g-m}$ as the output current.
The squarer/divider is obtained after few modifications by taking a copy of $I_1$ as the output, and considering $I_2$ and $I_3$ as the inputs. Figure 9 shows the complete circuits of the geometric-mean and squarer/divider blocks. Transistors M1A to M3A and also M1B to M3B form the voltage translinear loops and the remaining transistors are employed for injecting the proper currents into the translinear loops. As the figure shows, the sources of the translinear FG-MOSs are connected to the substrate, so the body effect is eliminated. Also the figure shows the minimum supply voltage of the circuit is one $V_{gs}$ plus one $V_{ds}$, and since extra biasing currents and voltages for the translinear loops are not needed, the static power consumption is decreased. The complexity of this circuit is lower than those of previously reported up-down translinear circuits [8-10].

It should be noted that the cascading of the squarer/divider and geometric-mean of Fig. 9, which will be applied to the circuit of Fig. 3, is accomplished by connecting the gate of transistor M5A to the gate of the transistor M5B. In such case transistors M4A and M4B will be eliminated.

### 3.3 Current-Splitter circuit

Class-AB SRD filters require the current splitter to split the input current into its differential form ($I_{inp}$ and $I_{inn}$). Ideally, a rectifier can be used, but in practice this will generate a large harmonic content that has to be cancelled at the output when taking the difference between the two output currents. For this reason, constant geometric-mean law [4, 12] in which signals $I_{inp}$ and $I_{inn}$ are related to $I_n$ by:

$$I_n = I_{inp} - I_{inn}$$

$$I_{inp} + I_{inn} = I_{ref}^2$$

is employed. $I_{ref}$ is the reference current and can be chosen arbitrary small in order to optimize both power consumption and signal-to-noise ratio. Figure 10 shows the circuit diagram of the splitter, in which, by employing the squarer/divider presented in Section 3, Eq. (31) is implemented by taking a copy of $I_1$ as the $I_{inn}$, $I_2$ as the $I_{inp}$ and $I_{gm}$ as the $I_{ref}$. Eq. (30) is also implemented using two MOS transistors MC1 and MC7.

### 4 Second-Order effects

The expressions presented in Section 3 are valid if the influences of the second-order effects that cause deviations from the ideal square-law behaviour of MOS (or FG-MOS) transistors are negligible. The body effect is defined as the change in the threshold voltage $V_{th}$ caused by source-to-substrate bias of MOS transistors. As have been already mentioned, since the sources of all transistors in the electronically simulated translinear loop is connected to the power or ground, the body effect is completely eliminated.

The channel-length modulation causes the drain current to be dependent on the drain voltage and its dependency is inversely proportional to the channel length. Long channel transistors have been employed in our proposed circuit to eliminate this effect. These large lengths also reduce the mobility degradation effects.

Contribution of parasitic capacitors $C_{gs}$, $C_{gd}$ and $C_{gb}$ in FG-MOSs has minor effect on the operation of the converter by choosing the input capacitances much larger than the parasitic capacitors. Fabrication tolerance can lead to mismatch between transistor parameters. The ability to program the charge on the gate of each FG-MOS allows for the cancellation of mismatch between the devices [17]. The decreasing and increasing of the charge of the floating gate can be accomplished by employing electron injection and tunnelling mechanism, respectively [18].
5 Simulation results
A second-order low-pass current-mode class-AB filter based on the block diagram of Figs. 4 and 6, and the proposed translinear loop of Fig. 8 was designed. The filter was simulated using HSPICE and BSIM3v3 model with TSMC 0.35um CMOS process parameters. Table 1 shows some parameters of the process. Supply voltage 1.2V and external capacitance 1nF were employed and all input capacitance ratios of FG-MOS transistors (\(w_i/C_i\)) were equal to 1/2. The aspect ratios of the NMOS and PMOS transistors were chosen 50um/3um and 150um/3um, respectively. For the transistors M3Ai in the geometric-mean blocks and M3Bi in the squarer/divider blocks the aspect ratio was 200um/3um. Most SPICE simulators have convergence problem with floating nodes during operating point calculations, so the N-input FG-MOS model of reference [16] is used. The proposed filter is tunable both in its frequency and quality factor. Figure 11 shows the frequency tuning plot, where the values of \(I_{b1}\) and \(I_{b2}\), equally, have been changed from 10uA to 90uA (plots left to right accordingly). In a similar way the quality factor tuning is achieved in constant \(\omega_0\), by multiplication of the bias current \(I_{b1}\) by a value, and division of the bias current \(I_{b2}\) by the same value. Figure 12 shows the quality factor tuning in frequency response using bias currents of 15uA, and five different values, changing linearly from 1 to 2 (plots down to up accordingly). Figure 13 shows the nonlinear behaviour of the output current using Total Harmonic Distortion (THD) results of a 4096 point Fast Fourier Transform (FFT). It shows the input current range of up to 75uA with less than -40dB THD in the output. Also with supply voltage 1.2V a dynamic range of 46dB at 1% THD is achieved which is 8dB more than the previously reported value for class-A square-root-domain filters [5, 19]. This improvement in dynamic range is due largely to the use of class-AB topology.

![Fig. 10 Circuit diagram of the splitter.](image)

![Fig. 11 \(\omega_0\) tuning in the frequency response.](image)

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6 Conclusion
By using of FG-MOS transistor operating in saturation region, a current-mode geometric-mean structure for low voltage class-AB square-root domain filters is presented. The proposed circuit is immune from body effect, has low complexity and low nonlinearity. Simulation results of a second-order LPF show the validity and effectiveness of the proposed technique.

References


Ebrahim Farshidi was born in Shoushtar, Iran, in 1973. He received the B.Sc. degree in 1995 from Amir Kabir University, Iran, and the M.Sc. degree in 1997 from Sharif University, Iran both in electronic engineering. He worked for Karun Pulp and Paper Company during 1997–2002. From 2002 he has been with shahid chamran university, Ahvaz as an Instructor in the Department of electrical engineering. He is currently working towards the Ph.D. degree in electrical engineering at IUT. His interest is in current-mode circuits design.

Sayed Masoud Sayedi was born in Maragheh, Iran, in 1960. He received the B.Sc. and M.Sc. degrees in electrical engineering from Isfahan University of Technology (IUT), and the Ph.D. degree in electronics from Concordia University in 1986, 1988, and 1996, respectively. From 1988 to 1992, and then since 1997, he has been with IUT, where he is currently an assistant professor in the Department of Electrical and Computer Engineering. His areas of interest include VLSI fabrication processes, low power VLSI circuits, and data converters.